

What is claimed is:

- 1 1. A logic synthesis method for reducing the delay of a
2 timing critical path in a circuit, comprising the steps of:
3 (a) selecting a gate which is not an inverter in the
4 timing critical path,
5 (b) swapping said timing critical path to a pin of said
6 gate,
7 (c) replacing said gate with a functionally equivalent
8 tapered gate,
9 (d) performing a timing analysis of said circuit , and
10 (e) if said timing analysis of said circuit
11 indicates improvement in a worst case delay through said
12 circuit,
13 (f) then retaining said tapered gate, and
14 (g) if said timing analysis of said circuit
15 indicates no improvement in said worst case delay through
16 said circuit,
17 (h) then swapping said tapered gate back to said
18 selected gate for use in said circuit.
- 1 2. The logic synthesis method of claim 1 wherein
2 said gate is selected from a gate library comprising a
3 set of non-tapered gates and a set of tapered gates, and
4 wherein in said gate library,
5 said non-tapered gates are characterized by a stack of
6 devices of the same width and said tapered gates are
7 characterized by a stack of devices of different widths.
- 1 3. The logic synthesis method of claim 1 wherein said gate
2 is selected from a gate library comprising a set of
3 non-tapered gates and a set of tapered gates,
4 and wherein each set in said gate library comprises one or
5 more of the following gates: NAND gates, NOR gates,
6 AND-OR-INVERT gates, and OR-AND-INVERT gates.

1 4. A logic synthesis method as in claim 3 whereby the delay
2 through said tapered gate and the delay through said
3 non-tapered gate are compared.

1 6. A logic synthesis method as in claim 1 whereby a
2 plurality of tapered gates exist for a non-tapered gate,
3 said plurality of tapered gates being functionally
4 equivalent to said non-tapered gate.

1 7. A logic synthesis method as in claim 6 whereby the
2 selection of said plurality of tapered gates available for
3 use in said circuit is swapped into said circuit for
4 comparison with a timing analysis of the circuit.

1 8. A logic synthesis method as in claim 7 whereby the delay
2 through said plurality of tapered gates and the delay
3 through said non-tapered gate are compared.

1 9. A logic synthesis method as in claim 8 whereby the gate
2 of said plurality of gates which yields the shortest delay
3 is the one retained for said circuit.